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ABSTRACT The programmable logic block (PLB) in a modern FPGA features a built-in carry chain (or adder) and a decompos-able LUT, where such an LUT may be

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decomposed into two or more smaller  
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a fault-tolerant logic resynthesis  
algorithm for LUT-based FPGAs which

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Technical Report No. UCB/ERL

M93/80 November 1993 <http://www2.e>

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[ecs.berkeley.edu/Pubs/TechRpts/1993/ERL-93-80.pdf](https://ecs.berkeley.edu/Pubs/TechRpts/1993/ERL-93-80.pdf). Field programmable logic devices (FPLDs) are fast emerging as viable alternatives to mask programmed parts because of their rapid time-to-market and low costs.

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